Attorney Docket No.: 042390.P7462D Patent

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applica	ation of:	)	
	Parat, Krishna et al.	) Examiner:	Not yet assigned
Serial No.:	Not yet assigned	) Art Unit:	Not yet assigned
Filed:	Herewith	)	
For: A NOVEL FLASH INTEGRATED CIRCUIT AND ITS METHOD OF FABRICATION Assistant Commissioner for Patents		) ) _)	
and Tradem	arks		
Washington,	, D.C. 20231		

### FORMAL DRAWINGS SUBMISSION

Enclosed herewith for submission in the United States Patent and Trademark Office are twelve (12) sheets of formal drawings for the patent application referenced above.

If there are any further charges please charge them to Deposit Account No. 02-2666. A duplicate of this sheet is enclosed for that purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

23 , 2001 Michael A. Bernadicou

Reg. No. 35,934

12400 Wilshire Boulevard Seventh Floor Los Angeles, California 90025-1026 (408) 720-8300

"Express Mail" mailing label number: \$6472746938US
Date of Deposit: MAY 33, 360 I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and

that this paper or fee has been addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231

(Typed or printed name of person mailing paper or fee)

Signature of person mailing paper or fee)

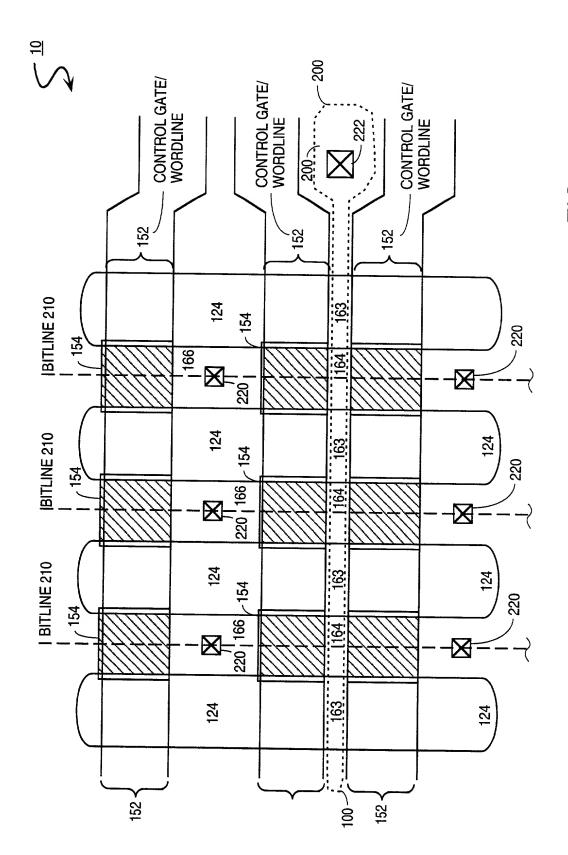
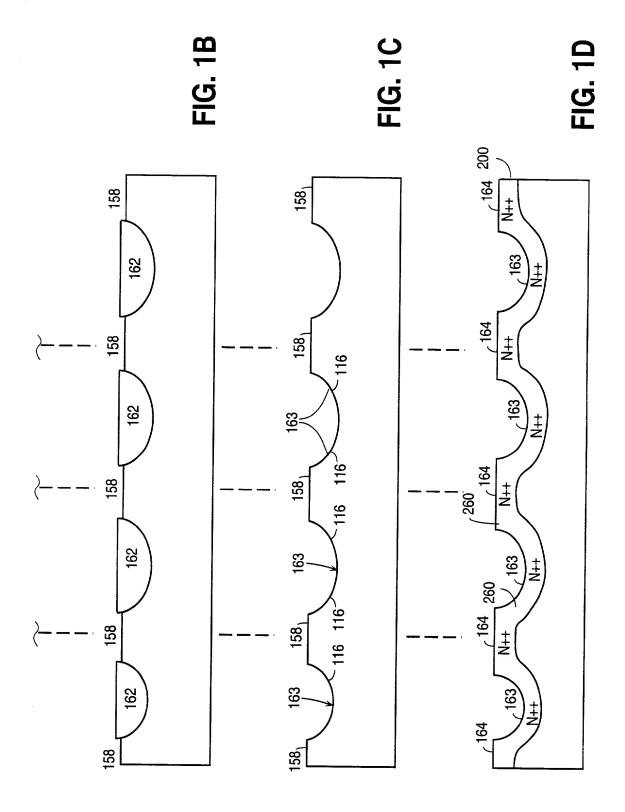


FIG. 1A



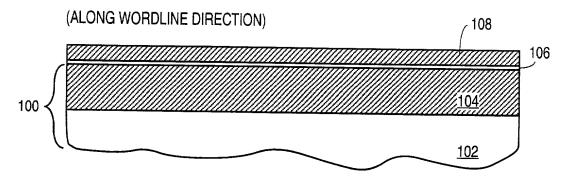


FIG. 2

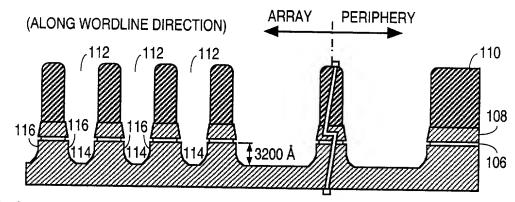


FIG. 3

(ALONG WORDLINE DIRECTION)

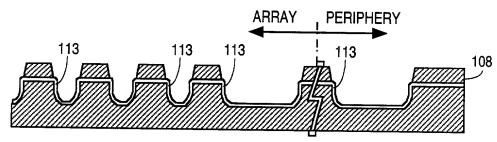


FIG. 4

(ALONG WORDLINE DIRECTION)

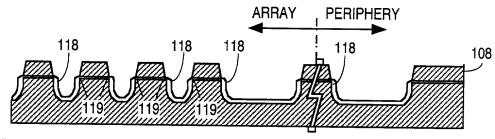


FIG. 5

(ALONG WORDLINE DIRECTION)

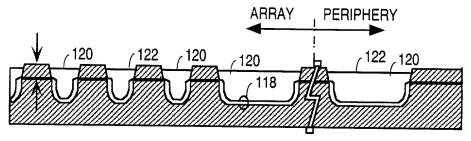


FIG. 6

(ALONG WORDLINE DIRECTION)

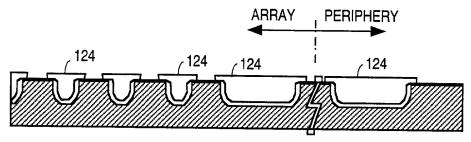


FIG. 7

(ALONG WORDLINE DIRECTION)

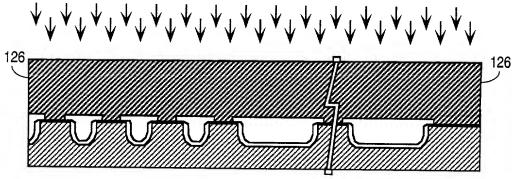


FIG. 8

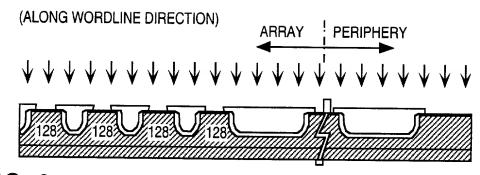


FIG. 9

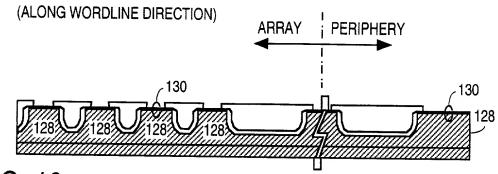


FIG. 10

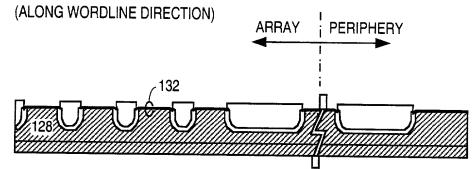


FIG. 11

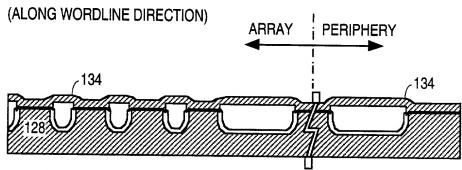
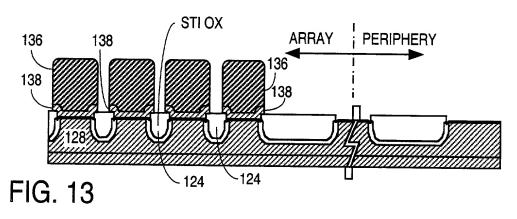
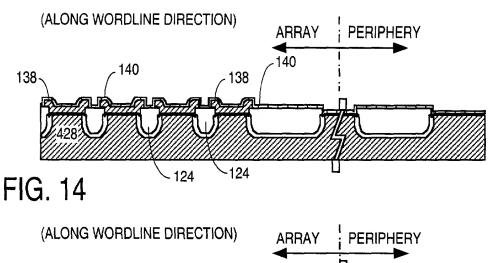


FIG. 12

(ALONG WORDLINE DIRECTION)





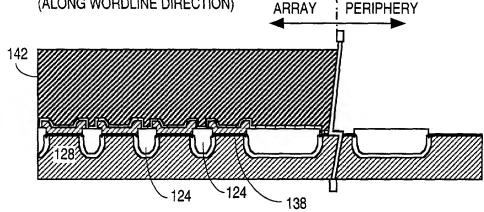


FIG. 15

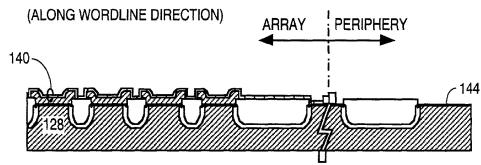


FIG. 16

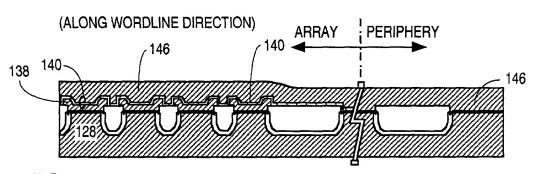


FIG. 17

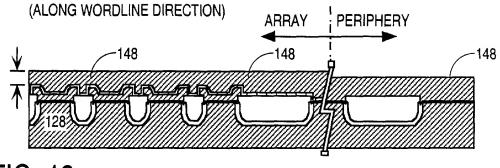


FIG. 18



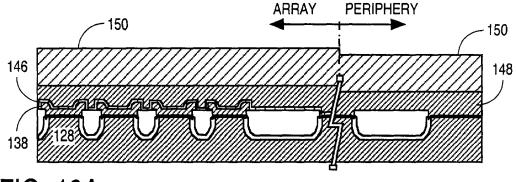


FIG. 19A

## **CROSS-SECTION ALONG BITLINE DIRECTION**

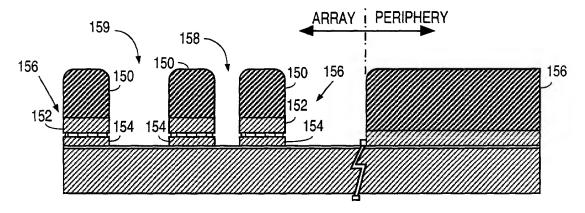


FIG. 19B

## THROUGH S/D IN BITLINE DIRECTION

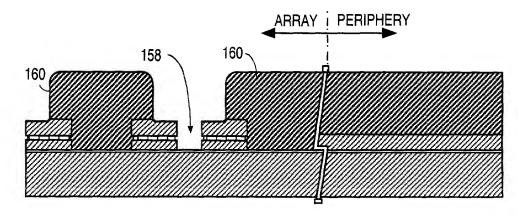
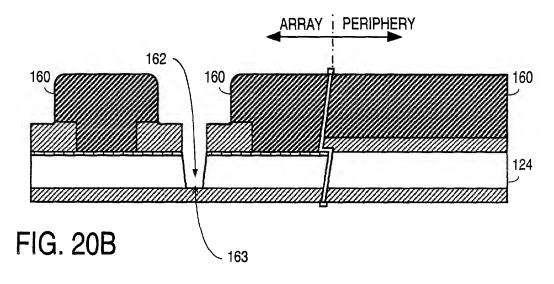


FIG. 20A

#### THROUGH STI IN BITLINE DIRECTION



#### ALONG BITLINE DIRECTION

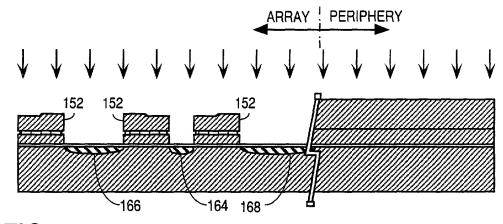


FIG. 21

# ALONG BITLINE DIRECTION

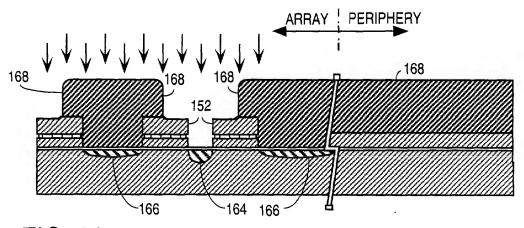


FIG. 22

# ALONG BITLINE DIRECTION

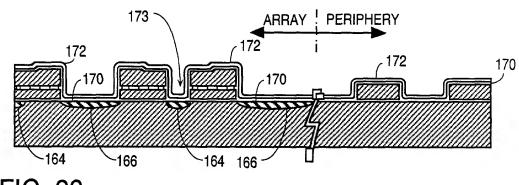


FIG. 23

## ALONG BITLINE DIRECTION

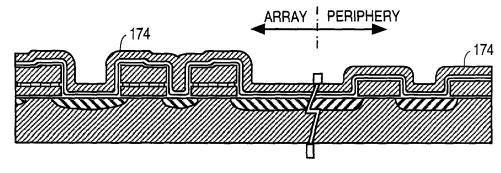


FIG. 24

# ALONG BITLINE DIRECTION

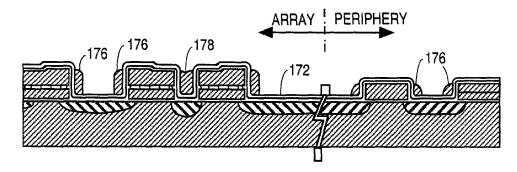


FIG. 25

#### ALONG BITLINE DIRECTION

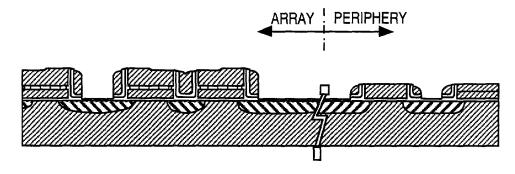


FIG. 26

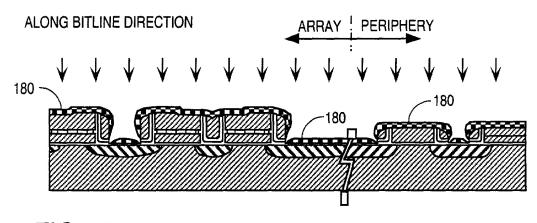
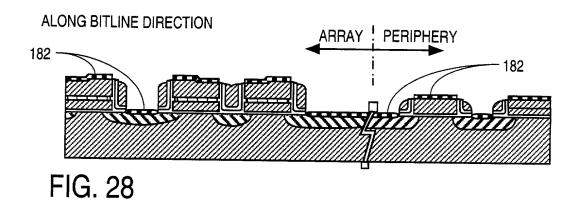


FIG. 27



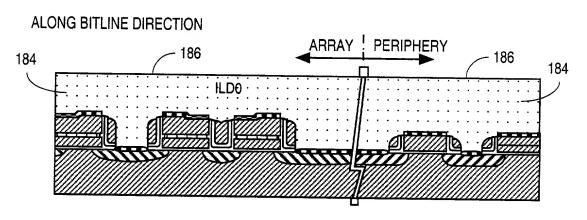
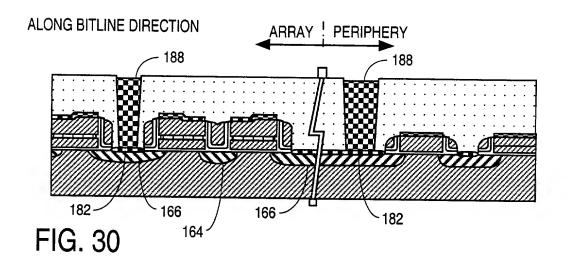


FIG. 29



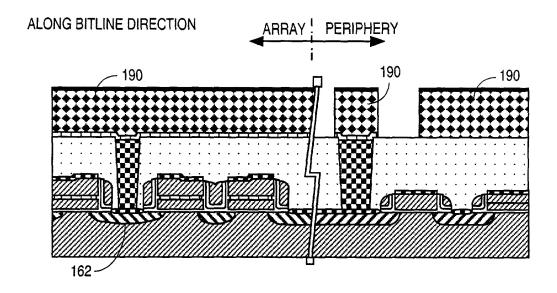


FIG. 31